USB2 DEVICE CONTROLLER CORE

OVERVIEW

The AL-USB2D-CTRL fully synthesizable core implements a complete high/full-speed (480/12Mps) peripheral controller that interfaces to a UTMI USB port transceiver on one side and to a system's microprocessor on the other. It is user-configurable for up to 15 IN and OUT endpoints, and includes power management and remote wake-up functions.

Options include a protocol aware DMA controller, support for a variety of widely used bus interfaces, and a UTMI Low Pin Interface (ULPI).

Designed for easy reuse in ASIC and FPGA implementations, the microcode-free design is strictly synchronous with positive-edge clocking, no internal tri-states and a synchronous reset; therefore scan insertion is straightforward. The core has been optimized and silicon proven on Xilinx and Altera FPGAs.

APPLICATIONS

The AL-USB2-CTRL IP core can be used as a cost effective high speed data transfer solution for applications including

- Embedded microcontroller systems
- Communication & networking systems
- Digital Media controllers

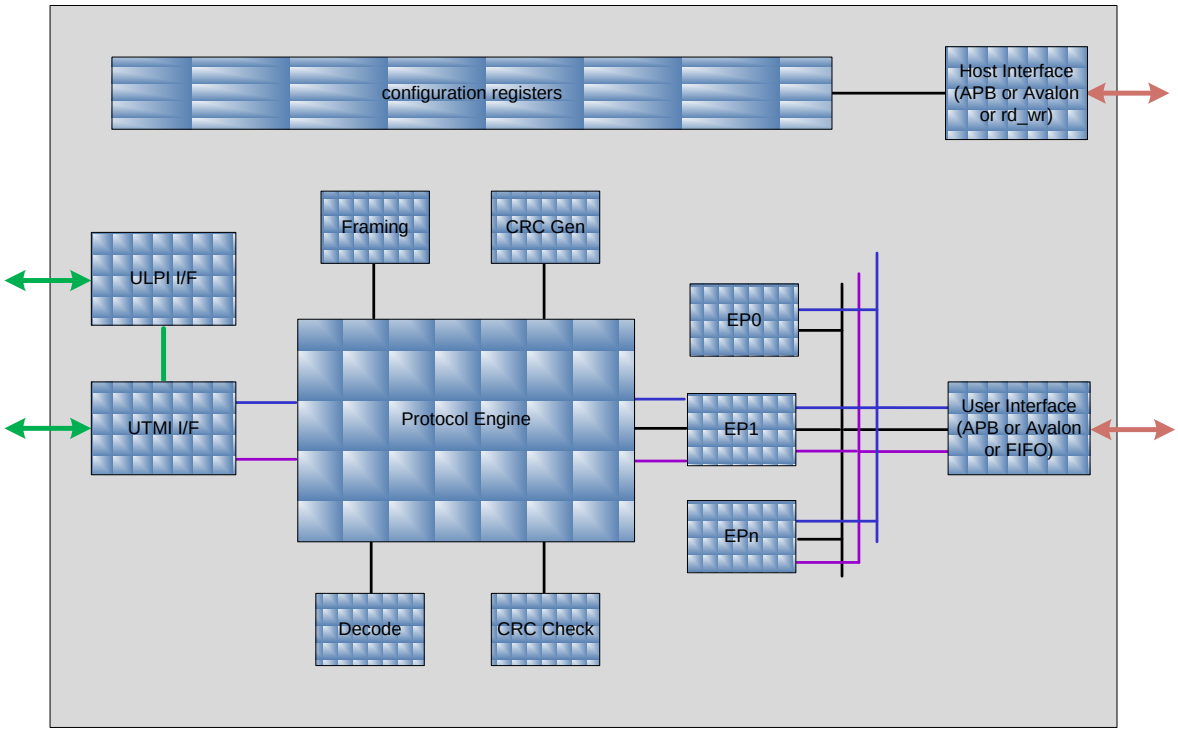
SOFTWARE

As a one stop complete solution, software stack with most popular device classes are also available. It has been designed for portability in a variety of embedded applications. It includes an intuitive Application Programming Interface (API) for application development.

FEATURES

- ✓ USB 2.0 compliant device.
- ✓ ULPI/ UTMI interface to the external PHY
- ✓ 32bit Avalon or AHB slave interface to application.
- ✓ Supports high speed (480Mbps), full speed (12Mbps) bit rates.
- ✓ Supports Control, Bulk, Interrupt and Isochronous transfers.
- ✓ Remote wake-up function capable.
- ✓ Performs CRC check/generation.
- ✓ Performs PID verification, address recognition and handshake evaluation and response.
- ✓ Decodes and handles standard USB commands.
- ✓ Endpoints, their parameters and FIFO densities are configurable.
- ✓ Preconfigured for 3 endpoints (control, bulk in, bulk out)
- ✓ Software/ Hardware controlled enumeration.
- ✓ Compact plug-in solution for SOC applications.

BLOCK DIAGRAM



IMPLEMENTATION RESULTS

DEVICE	AREA	RAM	FREQUENCY
ALTERA CYCLONE III	~1032 LCs	2 M9Ks	60 MHz
XILINX VIRTEX 4	~711 Slices	2 BRAMs	60 MHz

DELIVERABLES

- HDL RTL source code (ASICs) or post-synthesis EDIF netlist (FPGAs)
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001) including external FIFOs, buffers, models of interfaces, vectors for testing the core, and the core
- Simulation script, vectors, expected results, and comparison utility
- Synthesis script (ASICs) or place and route script (FPGAs)
- Comprehensive user documentation, including detailed specifications and a system integration guide

ORDERING INFORMATION

Please contact the following office for pricing and licensing questions.

Atria Logic, Inc.
341 Cobalt Way Ste.204
Sunnyvale, CA 94085
Ph: 408.730.4100
Fax: 408.730.4101
Email: sales@atrialogic.com
http://www.atrialogic.com