H.264 BP VIDEO DECODER SYSTEM REFERENCE DESIGN ON ALTERA FPGA

OVERVIEW

The AL-H264D-REFD reference design is System-on-Chip (SoC) implementation of H.264/AVC Baseline Profile Decoder with an ARM Cortex-M1 or an Altera NIOS embedded processor along with peripheral logic. This reference design is implemented on Altera Cyclone-III FPGA development board.

Atria Logic offers complete set of IP cores to fasten development of H.264 Video Decoder System on ASIC or FPGA.

H.264 video processing is fairly complex and computationally intensive. Besides the memory bandwidth needs, the video processing requires constant inflow of bitstream data and outflow of decoded data either to be stored or displayed. This reference design is build using various IP's that would accommodate a video decoding demo. In this particular reference design apart from the H.264/AVC Baseline Profile Decoder the design has a multi-port DDR controller, an Ethernet MAC for input bitstream, Flash controller to access alternate bitstream from onboard flash, an ARM processor for control of all the IP and a LCD display controller to output the decoded pixels. Other than the ARM processor all the other IP is designed by Atria Logic (please refer to the product documentation for all the IP mentioned here and various other IP developed by Atria Logic at www.atrialogic.com).

Designed for easy reuse in ASIC and FPGA implementations, the design is strictly synchronous with positive-edge clocking. The implementation is completely programmable SoC solution. It is operable both in micro-code free hardwire mode or in SW assist mode in ARM/NIOS embedded processor system.

Features

- ✓ Implement low cost H.264 BP Video Decoder Reference Design on Altera Cyclone III.
- ✓ System on Chip design implemented with an ARM Cortex-M1 or Altera NIOS processors.
- ✓ H.264 BP Decoder is low power, low gate count implementation. Only 12 MHz is required to decode CIF resolution H.264 input stream at 30 fps.
- ✓ Video Decoder implementation can be HW-only, SW-only or mix. The design is stateless, and therefore supports multiple video streams at higher clock rates.
- ✓ On-chip peripherals include multi-port DDR1/2, USB2.0 Device, Ethernet MAC, LCD, Flash Controllers.
- ✓ All peripherals connect to processor bus fabrics using AMBA AHB or Altera Avalon interfaces.
- ✓ Single 50MHz clock source on the board. Two on-chip PLLs used to generate multiple internal clocks.
- ✓ Clock gating techniques employed on-chip. Clocks and resets are also under software control.
- ✓ FPGA Design easily portable to ASIC.

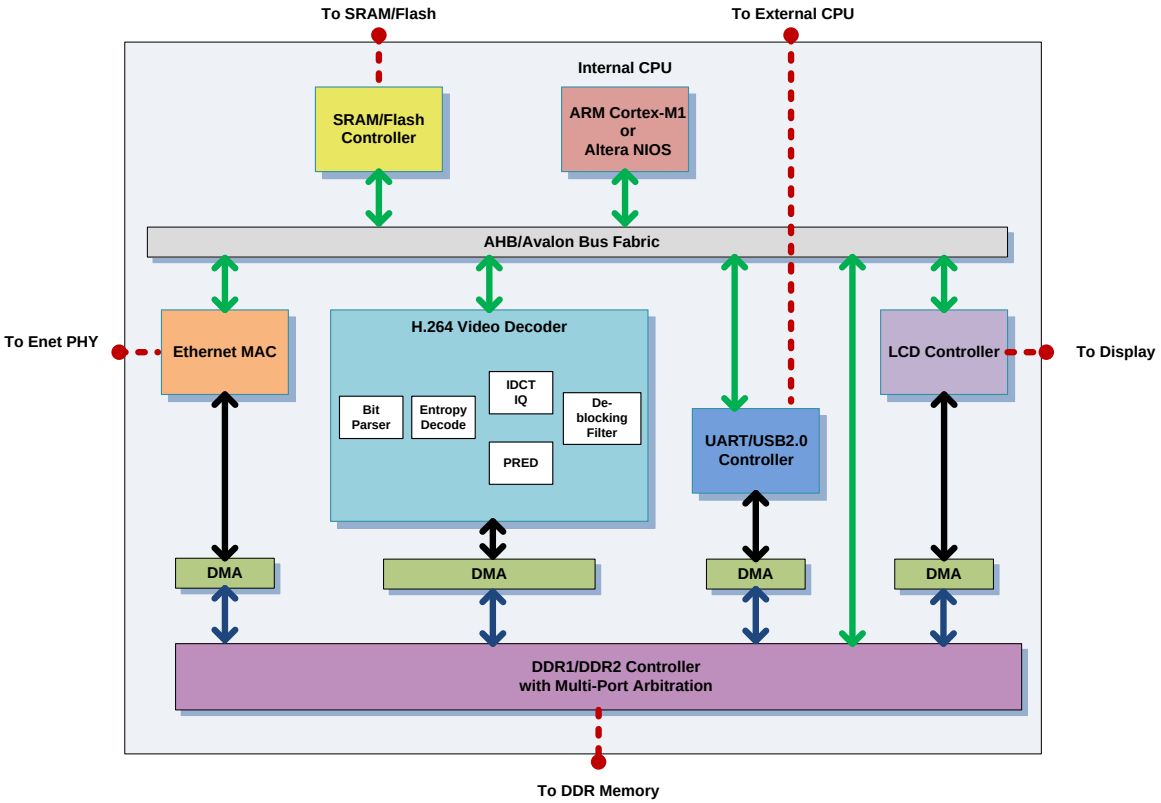
APPLICATIONS

- Mobile phone, Handheld video
- Camera, Security systems
- Video game consoles, Mobile TV
- Blu-ray DVD players
- Satellite TV/IPTV/Cable Set-top-box
- Video conferencing
- HD enabled MID, netbook

SOFTWARE

Control plane software is available for the IP core when run in HW-SW mode. It can be easily ported to any other embedded CPU. Also, the entire H.264 SW decoder is available as a separate product.

BLOCK DIAGRAM



PLATFORM

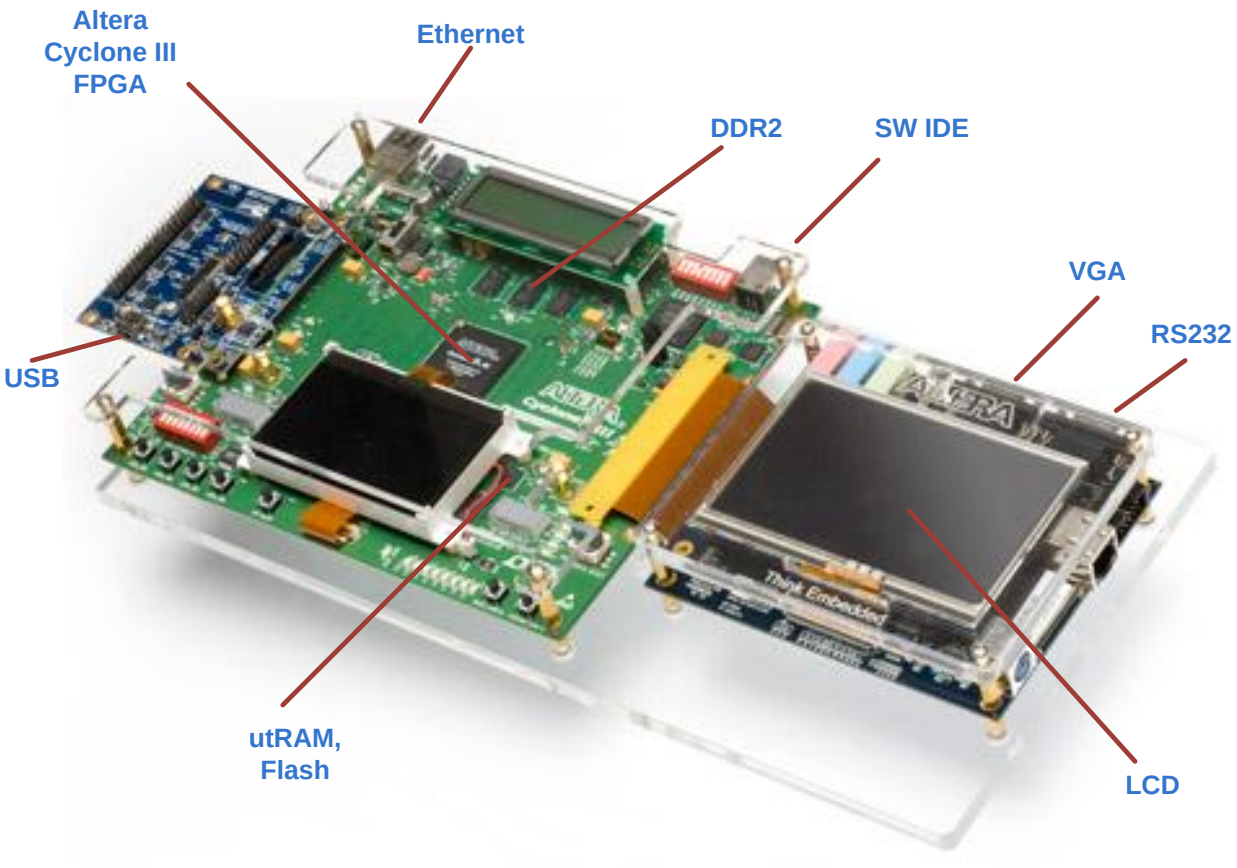
Atria Logic has implemented SoC design on Cyclone-III FPGA to demonstrate streaming H.264 video player, using off the shelf hardware development kits. The kit sources are:

- Altera Cyclone-III Development Kit: DK-DEV-3C120N
- Terasic MTDB (Multimedia Touch Panel Daughter Board)
- Terasic THDB-SUM (HSMC to Santa Cruz/ USB / Mictor Daughter Board)

Information on these development boards can be obtained from altera.com and terasic.com websites.

Below figure illustrates how the three boards are assembled together. Note that for this streaming video decoder demonstration, the Terasic THDB-SUM board is not necessary because the USB2.0 interface isn't involved for the demo. Therefore the reference design will work with just the Altera Kit and the Terasic MTDB daughter card.

The reference design demonstrates streaming video bitstream that comes through the highlighted Ethernet port. The decoded CIF frames are displayed only on the LCD.



CUSTOMIZATION

Atria Logic can customize the reference platform with any embedded processors besides ARM and Altera CPU. Video resolutions larger than CIF (352x288) can be displayed on the VGA port. Other FPGA devices are also supported. Please contact us for any custom implementations.

IMPLEMENTATION

The reference design is implemented on Altera Cyclone-III FPGA. Device utilization details are:

DEVICE	AREA	ON-CHIP RAM	PERFORMANCE
Cyclone III EP3C120	90K Logic Cells	60 Kbits	Fmax = 120 MHz

DELIVERABLES

- POF file containing two variant bit-files, which can be directly programmed to on board FLASH.
- SW to stream H.264 encoded bitstream over the Ethernet.
- Object file of a H.264 encoder to encode video for streaming.
- Comprehensive user documentation, including detailed specifications, system requirements and operational instructions.

ORDERING INFORMATION

Please contact the following office for evaluation and licensing questions.

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