DDR I/II DRAM CONTROLLER CORE

OVERVIEW

The AL_DDR12_CTRL Memory Controller Core implements an efficient and pipelined interface to DDR-I and DDR-II SDRAM devices targeted for System-on-Chip (SoC) and FPGA platforms.

The memory controller core is fully configurable to accommodate all the features in the JEDEC specification. The design has set of programmable registers to define the functionality of the memory controller and to configure the DRAM. On power-up the controller performs initialization of the DRAM based on the programmed paramerters in the registers. On completion of the initialization sequence, the DRAM will be ready to process READ/WRITE requests from the user. In case of multiple port access, an efficient Arbiter is used with programmable management scheme to have a fair arbitration. The controller also provides logic to support low-power applications by implementing SELF REFRESH and POWER-DOWN modes.

The controller core has the following modules:

- Control and Timing Engine
- DRAM Initialization Engine
- Command Generation Engine
- Address Generation and Bank Management
- Refresh Generation Engine
- Multiport Weighted Round-robin Arbiter
- Write Path and Read Capture Logic
- Calibration Logic
- PHY Logic for DDR I/O

The AL_DDR12_CTRL Core is designed for performance with low latencies and maximum bandwidth allocation for up to 16 requestors.

The AL_DDR12_CTRL Core is highly configurable allowing the user with several options such as: DRAM width, DRAM instance count, DRAM speed grade, DRAM CAS latencies, number of user ports for DRAM access.

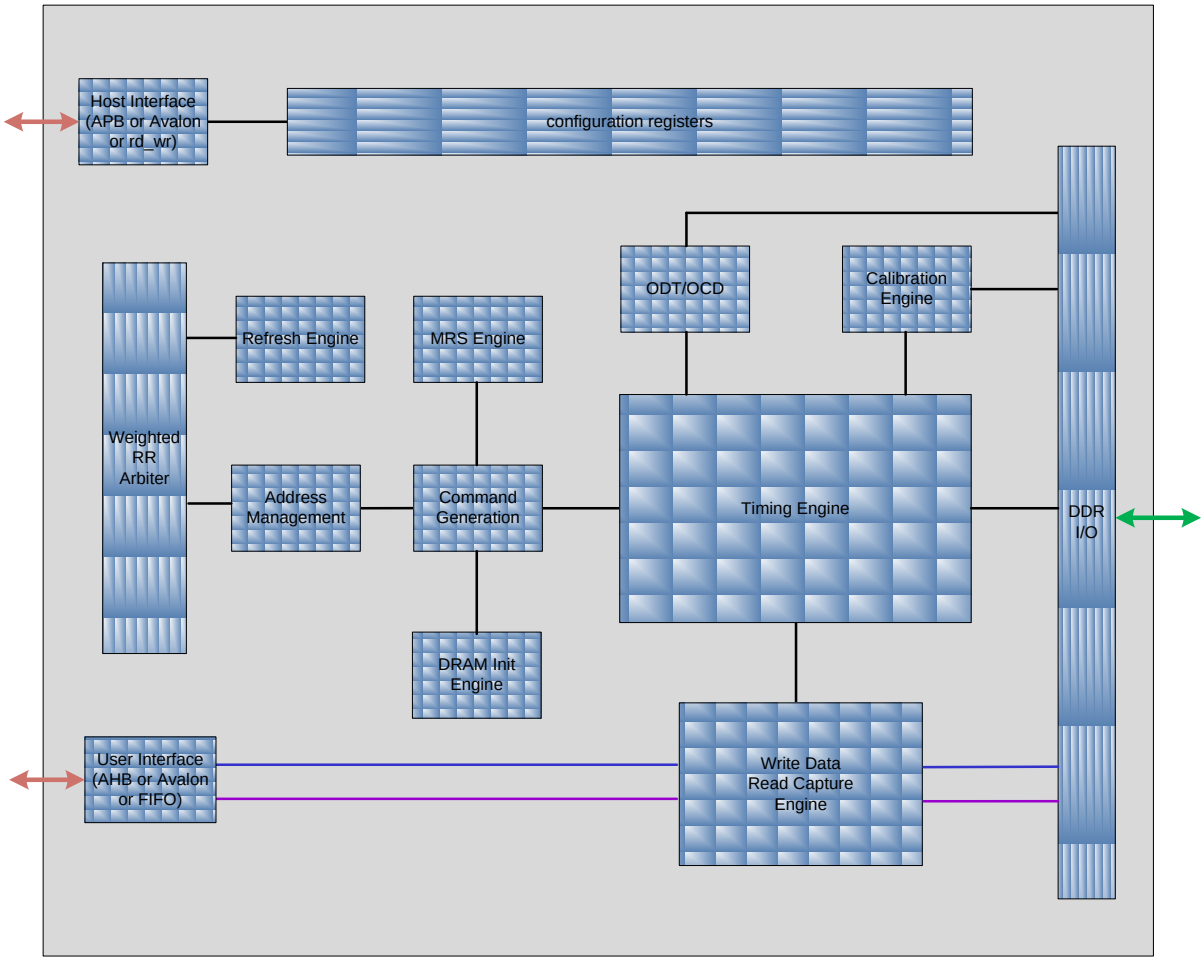
The Controller Core flexible user interfaces such as: Command/Data FIFO or AMBA-AHB or Altera Avalon Slave interfaces for easy SoC integration.

Features

- ✓ Compliant with JEDEC Standard.
- ✓ Support up to 4 Gb and 8 banks of DDR2 devices.
- ✓ Application bus – FIFO, AHB, Avalon. Support multiple agents on application bus interface with built-in credit/aging based weighted round robin arbitration scheme.
- ✓ Programmable CAS latency and DRAM timing parameters.
- ✓ Programmable auto-refresh time interval.
- ✓ Support power down, self refresh.
- ✓ Auto initialization of memories.
- ✓ Configurable address mapping between application and DRAM bank/row/column address.
- ✓ Auto-calibration scheme for DDIO interfaces, support for on-die termination and off chip driver impedance adjustment.
- ✓ Support back to back WR, RD commands with min timing.
- ✓ High data rate of memory throughput
- ✓ Choice of 16/32/64 DDR bus widths

The Core has been verified thoroughly with maximum test coverage and is proven on Altera and Xilinx FPGA platforms.

BLOCK DIAGRAM



IMPLEMENTATION

The IP core is implemented in Altera Cyclone-III and Xilinx Virtex 4 FPGA devices. Device utilization details are:

DEVICE	AREA	PERFORMANCE
ALTERA CYCLONE III	2500 LC	Fmax = 166 MHz
XILINX VIRTEX 4	1200 LC	Fmax = 166 MHz

DELIVERABLES

- HDL RTL source code or EDIF netlist for FPGA
- Self-checking Testbench in Verilog.
- Simulation scripts, vectors, expected results, and comparison utility
- Synthesis and STA scripts.
- Comprehensive user documentation, including detailed specifications and a system integration guide

ORDERING INFORMATION

Please contact the following office for evaluation and licensing questions.

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