



I2C MASTER/SLAVE CONTROLLER CORE

OVERVIEW

I2C is a two-wire, bidirectional serial bus that provides simple and efficient data transfer between devices. It uses serial data line (SDA) and serial clock line (SCL) for data transfers.

The Controller core interfacing to I2C bus can be easily integrated to an embedded system via AHB, APB, Avalon bus fabrics or custom logic via simple register programming. The system can request the controller to perform I2C data transfers and also poll status. The core serializes system transmit data of 8, 16, 32 or 64 bytes on the SDA IO pin. It also de-serializes system receive data.

In the master mode, the system can initiate write or read data transfer to the slave by programming the memory mapped registers within the Controller core. Byte transfers can be single or bursts (programmable size) based on the control writes to registers.

IMPLEMENTATION

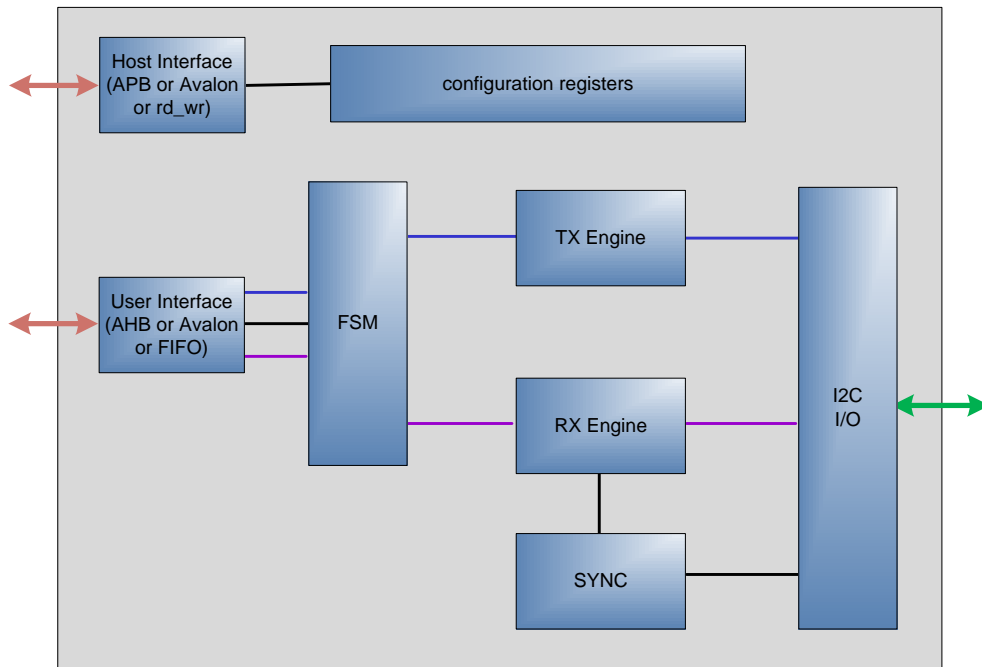
The IP core is implemented in Altera Cyclone-III and Xilinx Virtex 4 FPGA devices. Device utilization details are:

DEVICE	AREA	PERFORMANCE
ALTERA CYCLONE III	700 LC	Fmax = 100 MHz
XILINX VIRTEX 4	360 LC	Fmax = 100 MHz

Features

- ✓ Compatible with Philips I2C Specification version 2.1.
- ✓ Bus transfer speed ranges are 100 Kbps (normal) to 400 Kbps (fast).
- ✓ Start, Stop, Repeated Start, Acknowledgment Generation.
- ✓ Start, Stop, Repeated Start, Bus Busy Detection.
- ✓ Multi-master mode arbitration lost detection with automatic transfer detection.
- ✓ Clock Synchronization during Arbitration.
- ✓ Operates from a wide range of reference clocks with programmable prescalers.
- ✓ Supports 8 and 10 bit addressing of I2C slaves.
- ✓ System data width of 8, 16, 32 or 64 bits.
- ✓ Configurable to operate in master or slave mode.
- ✓ Fully Synthesizable design.
- ✓ Static synchronous design with rising edge clocking and asynchronous reset.

BLOCK DIAGRAM



DELIVERABLES

- HDL RTL source code or EDIF netlist for FPGA
- Self-checking Testbench in Verilog.
- Simulation scripts, vectors, expected results, and comparison utility
- Synthesis and STA scripts.
- Comprehensive user documentation, including detailed specifications and a system integration guide

ORDERING INFORMATION

Please contact the following office for evaluation and licensing questions.



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