



## 10/100/1000 Mbps ETHERNET MAC CORE

### OVERVIEW

The AL\_EMAC\_CORE Ethernet MAC Core is hardware implementation of Ethernet protocol defined by IEEE 802.3-2005 Specification. This core transmits and receives Ethernet frames to and from Ethernet network in all three speeds 10/100/1000 Mbps. Both half-duplex and full-duplex mode of operation are supported at all three speeds. The core interfaces to an industry standard external PHY device through RGMII or GMII for Gigabit Ethernet and RGMII or MII for fast Ethernet.

This core is implemented in both Altera Cyclone-III and Xilinx Virtex-4 FPGA. This core also supports pause frame control based on user programmable register setting.

The core has the following modules:

- Transmitter
- Receiver
- MDIO (Management Data Input Output interface)
- RGMII, GMII and MII interface
- Optional Read and Write DMA Engine
- Configuration and Status Registers for Tx, Rx and MDIO
- PHY Logic for Ethernet I/O

### IMPLEMENTATION

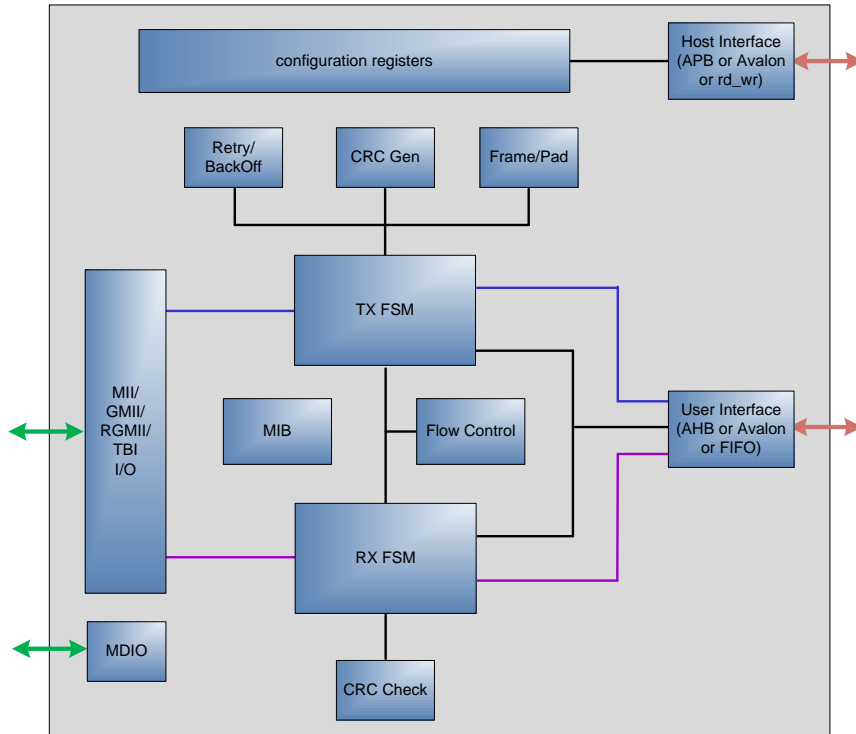
The IP core is implemented in Altera Cyclone-III and Xilinx Virtex 4 FPGA devices. Device utilization details are:

DEVICE	AREA	PERFORMANCE
ALTERA CYCLONE III	2000 LC	Fmax = 125 MHz
XILINX VIRTEX 4	900 LC	Fmax = 125 MHz

### Features

- ✓ Designed according to IEEE 802.3-2005 Specification.
- ✓ Support 10/100/1000 Mbps Ethernet MAC Speed in Half-duplex and Full-duplex mode.
- ✓ Promiscuous receive mode support.
- ✓ Untagged frames support.
- ✓ Support for Reduced Gigabit Media Independent Interface (RGMII) in all three speeds 10/100/1000 Mbps.
- ✓ Support for Gigabit Media Independent Interface (GMII), Media Independent Interface (MII).
- ✓ Support for Management Data Input Output (MDIO) interface to access configuration and status registers in PHY device.
- ✓ Supports for Pause Frame control from internal receive buffer and external CPU.
- ✓ Optional Programmable IFG value.
- ✓ CRC generation and checking both on transmit side and receive side.
- ✓ Option for user FCS field passing.
- ✓ Automatic padding on transmit side and option for remove padding on receive side.
- ✓ Support for read and write DMA engines for DDR memory.

## BLOCK DIAGRAM



## DELIVERABLES

- HDL RTL source code or EDIF netlist for FPGA
- Self-checking Testbench in Verilog.
- Simulation scripts, vectors, expected results, and comparison utility
- Synthesis and STA scripts.
- Comprehensive user documentation, including detailed specifications and a system integration guide

## ORDERING INFORMATION

Please contact the following office for evaluation and licensing questions.



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